(Pages : 2) **8803**

Reg. No. : .....

Name : .....

Fifth Semester B.Tech. Degree Examination, December 2015
(2008 Scheme)
08.505 : MICROPROCESSORS AND INTERFACING (R)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions. **Each** question carries **4** marks.

1. Explain the following 8085 microprocessor signals.
   a) RST 7.5
   b) IO/$\overline{M}$.
2. Explain flag register of 8085 microprocessor.
3. Explain the following addressing modes of 8085 with suitable examples.
   a) Register indirect addressing
   b) Implicit addressing.
4. Compare memory mapped I/O with I/O mapped I/O.
5. Write an 8086 based assembly language program to find the largest of 3 bytes of data.
6. Explain the following 8086 microprocessor instructions with examples.
   a) ROL
   b) IDIV.
7. What are assembler directives ? Give examples.
8. Give the control word format of 8254 chip.
9. How is the INTR pin enabled in the strobed input mode of operation of 8255 ?
10. Explain the DMA operation in its master mode.

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PART – B

Answer **any one** question from **each** Module :

Module – I

11. a) Explain the architecture of 8085 microprocessor with a neat diagram. 12

    b) With suitable diagram, explain how address bus, data bus and control signals are generated in 8085 microprocessor based system. 8

OR

12. a) Draw the timing diagram of opcode fetch machine cycle of 8085 microprocessor. Explain the activities in each T state. 10

    b) Give an interfacing circuitry to interface 2K bytes of EPROM and 1K byte of RAM to the 8085 microprocessor. Give the address map of the proposed design. 10

Module – II

13. a) Explain the Register Organization of 8086 microprocessor. 10

    b) Explain the physical memory organization in 8086 based system. 10

OR

14. a) Describe the functions of 8086 queue. How does the queue speed up processing ? 8

    b) Draw and explain the block diagram of 8259A priority interrupt controller. Explain the interrupt operation and its priority modes. 12

Module – III

15. a) Draw and explain the block diagram of 8251 A USART and its asynchronous mode of operation. 10

    b) Give an interfacing circuit to interface 8254 chip with 8086 processor. Determine the base address for the chip, the counters and control word register. 10

OR

16. a) Draw and explain the architecture of 8237 DMA controller. 10

    b) Explain different ports and different modes of operation of 8255 chip. 10